CLAIMS

The invention claimed is:

1. A digital data apparatus comprising:

a semiconductive substrate comprising a node location configured to receive an electrical charge of a single bit of digital information;

a first capacitor coupled with the node location and configured to store a first portion of the electrical charge of the single bit of digital information, wherein the first capacitor comprises a first type of capacitive structure;

a second capacitor coupled with the node location and configured to store a second portion of the electrical charge of the single bit of digital information, wherein the second capacitor comprises a second type of capacitive structure different than the first type of capacitive structure; and

a transistor coupled with the node location and configured to control a flow of the first and second portions of the electrical charge of the single bit of digital information with respect to the node location and respective ones of the first and the second capacitors.

2. The apparatus of claim 1 wherein a substantial portion of a storage component of the first capacitor is elevationally above a horizontal reference line and a substantial portion of a storage component of the second capacitor is elevationally below the horizontal reference line.

3. The apparatus of claim 2 wherein the horizontal reference line comprises a surface of the semiconductive substrate.

4. The apparatus of claim 1 wherein the first type of capacitive structure comprises a stacked capacitor, and the second type of capacitive structure comprises a trench capacitor.

5. The apparatus of claim 1 wherein the first and the second capacitors comprise a cell configured to store the single bit of digital information.

6. The apparatus of claim 1 further comprising a common bitline, and wherein both of the first and the second capacitors are coupled with the common bitline via the transistor.

7. The apparatus of claim 6 wherein the first and the second capacitors comprise a first capacitor pair, and further comprising a second capacitor pair coupled with the bitline via another transistor.

8. The apparatus of claim 1 further comprising processing circuitry coupled with the bitline and configured to control a content of the single bit of digital information comprising one of a plurality of logical states.

9. The apparatus of claim 1 further comprising processing circuitry configured to access the single bit of digital information from the first and the second capacitors.

10. The apparatus of claim 1 further comprising processing circuitry configured to control writing of the single bit of digital information to the first and the second capacitors.

11. A digital data apparatus comprising:

a semiconductive substrate;

a first capacitor configured to store a first electrical charge, wherein the first capacitor comprises a first type of capacitive structure;

a second capacitor configured to store a second electrical charge, wherein the second capacitor comprises a second type of capacitive structure different than the first type of capacitive structure;

a common bitline configured to conduct the first and the second electrical charges; and

a plurality of transistors formed using the semiconductive substrate and coupled with the bitline, wherein the transistors are individually configured to control storage of a respective one of the first and the second electrical charges with respect to a respective one of the first and the second capacitors.

12. The apparatus of claim 11 wherein the first and the second electrical charges correspond to different bits of digital information.

13. The apparatus of claim 11 wherein the first and the second electrical charges correspond to a single bit of digital information.

14. The apparatus of claim 11 wherein the first type of capacitive structure comprises a stacked capacitor, and the second type of capacitive structure comprises a trench capacitor.

15. The apparatus of claim 11 wherein one of the first and the second capacitors comprises a trench capacitor, and a respective one of the transistors associated with the trench capacitor is formed below a surface of the semiconductive substrate adjacent a sidewall of a trench of the trench capacitor.

16. The apparatus of claim 11 further comprising processing circuitry coupled with the bitline and configured to individually control the first and the second electrical charges to individually correspond to one of a plurality of logical states.

17. A digital data apparatus comprising:

a semiconductive substrate;

a first capacitor configured to store a first electrical charge, wherein the first capacitor comprises a first type of capacitive structure;

a second capacitor configured to store a second electrical charge, wherein the second capacitor comprises a second type of capacitive structure different than the first type of capacitive structure;

a common conductive structure configured to effect storage of the first and the second electrical charges using respective ones of the first capacitor and the second capacitor; and

a plurality of transistors formed using the semiconductive substrate and individually associated with one of the first capacitor and the second capacitor.

18. The apparatus of claim 17 wherein the common conductive structure comprises a bitline configured to conduct the first and the second electrical charges.

19. The apparatus of claim 17 wherein the common conductive structure comprises a wordline configured to control an operation of the transistors.

20. The apparatus of claim 17 wherein the first type of capacitive structure comprises a stacked capacitor, and the second type of capacitive structure comprises a trench capacitor.

21. The apparatus of claim 20 wherein the stacked capacitor and the trench capacitor are individually configured to store a portion of a charge of a single bit of information.

22. The apparatus of claim 20 wherein the stacked capacitor and the trench capacitor are associated with separate bitlines and the common conductive structure comprises a common wordline.

23. The apparatus of claim 20 wherein the stacked capacitor and the trench capacitor are associated with separate wordlines and the common conductive structure comprises a common bitline.

24. The apparatus of claim 20 wherein the stacked capacitor and the trench capacitor comprise respective storage nodes associated with separate wordlines and separate bitlines forming two quasi independent memories.

25. A digital data apparatus comprising:

a semiconductive substrate comprising a plurality of node locations;

a first capacitor configured to store an electrical charge for a first bit of digital information, wherein the first capacitor comprises a first type of capacitive structure coupled with a first of the node locations;

a second capacitor configured to store an electrical charge for a second bit of digital information, wherein the second capacitor comprises a second type of capacitive structure different than the first type of capacitive structure and coupled with a second of the node locations;

a plurality of bitlines individually configured to conduct an electrical charge with respect to a respective one of the first and second node locations; and

a plurality of transistors coupled with respective ones of the bitlines, wherein the transistors are individually configured to control a flow of the respective electrical charges intermediate respective ones of the first and the second capacitors and the respective ones of the bitlines.

26. The apparatus of claim 25 wherein one of the first and the second capacitors comprises a trench capacitor, and a respective one of the transistors associated with the trench capacitor is formed below a surface of the semiconductive substrate adjacent a sidewall of a trench of the trench capacitor.

27. The apparatus of claim 25 wherein the first and the second capacitors are formed laterally adjacent to one another.

28. The apparatus of claim 25 wherein the first type of capacitive structure comprises a stacked capacitor, and the second type of capacitive structure comprises a trench capacitor.

29. The apparatus of claim 25 wherein the first and the second capacitors comprise independent storage devices configured to store the first and the second bits of digital information independent of one another.

30. The apparatus of claim 25 further comprising processing circuitry coupled with the bitlines and configured to individually control the first and the second bits of digital information into one of a plurality of logical states.

31. A digital data apparatus comprising:

substrate means having an associated horizontal reference line;

first storage means for storing a first electrical charge corresponding to a single bit of digital information, wherein the first storage means is positioned elevationally above the horizontal reference line;

second storage means for storing a second electrical charge corresponding to the single bit of digital information, wherein the second storage means is positioned elevationally below the horizontal reference line; and

control means for selectively communicating respective ones of the first and the second electrical charges with respect to respective ones of the first storage means and the second storage means.

32. The apparatus of claim 31 wherein the horizontal reference line is substantially parallel to a surface of the substrate means.

33. The apparatus of claim 31 wherein the horizontal reference line comprises a surface of the substrate means.

34. The apparatus of claim 31 wherein the first storage means comprises a stacked capacitor and the second storage means comprises a trench capacitor.

35. A digital data apparatus comprising:

memory comprising:

a semiconductive substrate;

a trench capacitor configured to store a first electrical charge;

a stacked capacitor configured to store a second electrical charge;

a common bitline configured to conduct the first and the second electrical charges; and

a plurality of transistors formed using the semiconductive substrate and coupled with the bitline, wherein the transistors are individually configured to control storage of a respective one of the first and the second electrical charges with respect to a respective one of the first and the second capacitors; and

processing circuitry electrically coupled with the memory and configured to control the generation of the first and the second electrical charges.

36. A digital data operational method comprising:

providing a plurality of capacitors comprising a plurality of different types of capacitive structures using a semiconductive substrate;

communicating an electrical charge corresponding to a single bit of digital information using a bitline;

storing the electrical charge of the single bit of digital information using plural

ones of the capacitors comprising different types of capacitive structures; and

controlling communication of the electrical charge intermediate the capacitors and the bitline using a transistor to read and write the bit of digital information with respect to the capacitors.

37. The method of claim 36 wherein one of the capacitors is formed elevationally above a horizontal reference line and an other of the capacitors is formed elevationally below the horizontal reference line.

38. The method of claim 37 wherein the one capacitor comprises a stacked capacitor and the other capacitor comprises a trench capacitor.

39. The method of claim 36 further comprising accessing the bit of digital information using processing circuitry configured to process the bit of digital information.

40. A digital data operational method comprising:

providing a plurality of capacitors comprising different types of capacitive structures using a semiconductive substrate;

communicating a plurality of electrical charges using a common bitline coupled with the capacitors;

storing one of the electrical charges from the bitline using one of the capacitors having a first type of capacitive structure; and

storing an other of the electrical charges from the bitline using an other of the

capacitors having a second type of capacitive structure different than the first type of capacitive structure.

41. The method of claim 40 wherein the one and the other electrical charges together comprise a single bit of digital information.

42. The method of claim 40 wherein the one and the other electrical charges comprise respective different bits of digital information.

43. The method of claim 40 wherein the providing comprises providing the one capacitor elevationally above a horizontal reference line and providing the other capacitor elevationally below the horizontal reference line.

44. The method of claim 40 wherein the one capacitor comprises a stacked capacitor and the other capacitor comprises a trench capacitor.

45. The method of claim 40 wherein the storings of the one and the other electrical charges individually comprise storing using a respective one of a plurality of transistors, and wherein one of the transistors is formed adjacent a sidewall of the other capacitor comprising a trench capacitor.

46. The method of claim 40 further comprising processing the electrical charges using processing circuitry.